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EXPRESS MAIL LABEL NO. EV669678858US

PATENTS
Attorney Docket No.: ELM-2 Cont. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Glenn J. Leedy
Application No.	:	10/672,961 Confirmation No.: 9439
Filed	:	September 26, 2003
For	:	THREE DIMENSIONAL MULTI LAYER MEMORY AND CONTROL LOGIC INTEGRATED CIRCUIT STRUCTURE
Group Art Unit	:	2822
Examiner	:	Monica Lewis

Director of the U.S. Patent
and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22313-1450

PETITION UNDER 37 C.F.R. §1.181(a)
TO WITHDRAW HOLDING OF ABANDONMENT
BASED ON EVIDENCE THAT
A REPLY WAS TIMELY MAILED OR FILED

Sir:

On October 10, 2006, the Patent and Trademark Office issued a Notice of Abandonment stating that the above-identified patent application has become abandoned for failure to timely file a proper reply to the Office Action mailed on March 28, 2006.

On September 26, 2006, however, applicant mailed, using the Certificate of Mailing procedure of 37 C.F.R. § 1.10, a Request for Continued Examination, a Petition Under 37 C.F.R. § 1.136(a) for Extension of Time (including permission to charge the fee to a Deposit Account), a Reply

to Office Action, and an Information Disclosure Statement. All of these documents were filed in response to the Office Action mailed March 28, 2006. The Petition for Extension of Time requested a three-month extension of time, extending the date for response to September 28, 2006. Thus, a timely reply was filed and the Notice of Abandonment was went in error.

A postcard receipt which itemizes and properly identifies the items which are being filed serves as *prima facie* evidence of receipt in the USPTO of all the items listed thereon on the date stamped thereon by the USPTO (see MPEP § 503). A copy of a return receipt postcard itemizing the above-mentioned submissions and date-stamped by the Patent and Trademark Office on September 26, 2006, is attached hereto as Appendix A. A copy of the Express Mail mailing label date-stamped by the USPS on September 26, 2006 and having the Express Mail number indicated on applicant's submissions of September 26, 2006, is attached hereto as Appendix B. For the Examiner's convenience, copies of the Express Mail Certification, Request for Continued Examination, Petition for Extension of Time, Reply to Office Action, and Information Disclosure Statement filed by the applicant on September 26, 2006 are attached hereto as Appendix C. Furthermore, the documents filed on September 26, 2006 are on the Patent Application Information Retrieval (PAIR) system of the USPTO and have been accorded a filing date of September 26, 2006. A copy of the front page of the Reply as downloaded from PAIR, that shows the OIPE stamp of September 26, 2006 is enclosed herewith as Appendix D.

Accordingly, applicant respectfully requests withdrawal of the holding of abandonment of this application pursuant to 37 C.F.R. §1.181(a).

On or about October 12, 2006, the undersigned left a telephone message to Examiner Lewis regarding the mailing of the Notice of Abandonment and explained that it was sent in error. On or about October 17, 2006, Examiner Lewis called the undersigned and the undersigned stated that applicant could file a petition to have the holding of abandonment sent in error in the application withdrawn. Examiner Lewis said she would look into the situation. On October 23, 2006, Examiner Lewis called Jeffrey C. Aldridge and requested that a petition be filed to have the holding of abandonment of the application withdrawn.

If necessary, this Request may be deemed a Petition for Revival of an Abandoned Application under 37 C.F.R. § 1.137(a) or (b), as may be deemed appropriate. This application was not intentionally abandoned. Moreover, any abandonment that may have occurred despite applicant having timely filed a response would inherently have been unavoidable.

The Commissioner is hereby authorized to charge any fees that may be due in connection with this Petition to Deposit Account No. 06-1075 (Order No. 001202-0127). A duplicate copy of this Petition is enclosed herewith.

An early and favorable action is respectfully requested.

Respectfully submitted,

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Appendix A

Copy of a return receipt postcard itemizing the submissions made by applicant on September 26, 2006 and date-stamped by the Patent and Trademark Office on September 26, 2006.

DOCKET NO. ELM-2 Cont. 4

CONFIRMATION NO. 9439

APPLICANT Glenn J. Leedy

APPLICATION NO. 10/672,961 FILED September 26, 2003

RECEIPT IS HEREBY ACKNOWLEDGED OF THE

Express Mail Certification and Request for Continued Examination (in duplicate); Reply to Office Action; Information Disclosure Statement (in duplicate); Form PTO/SB/08 (in duplicate); and copies of thirteen (13) cited references.

DATED September 26, 2006

FILED IN CONNECTION WITH THE ABOVE CASE

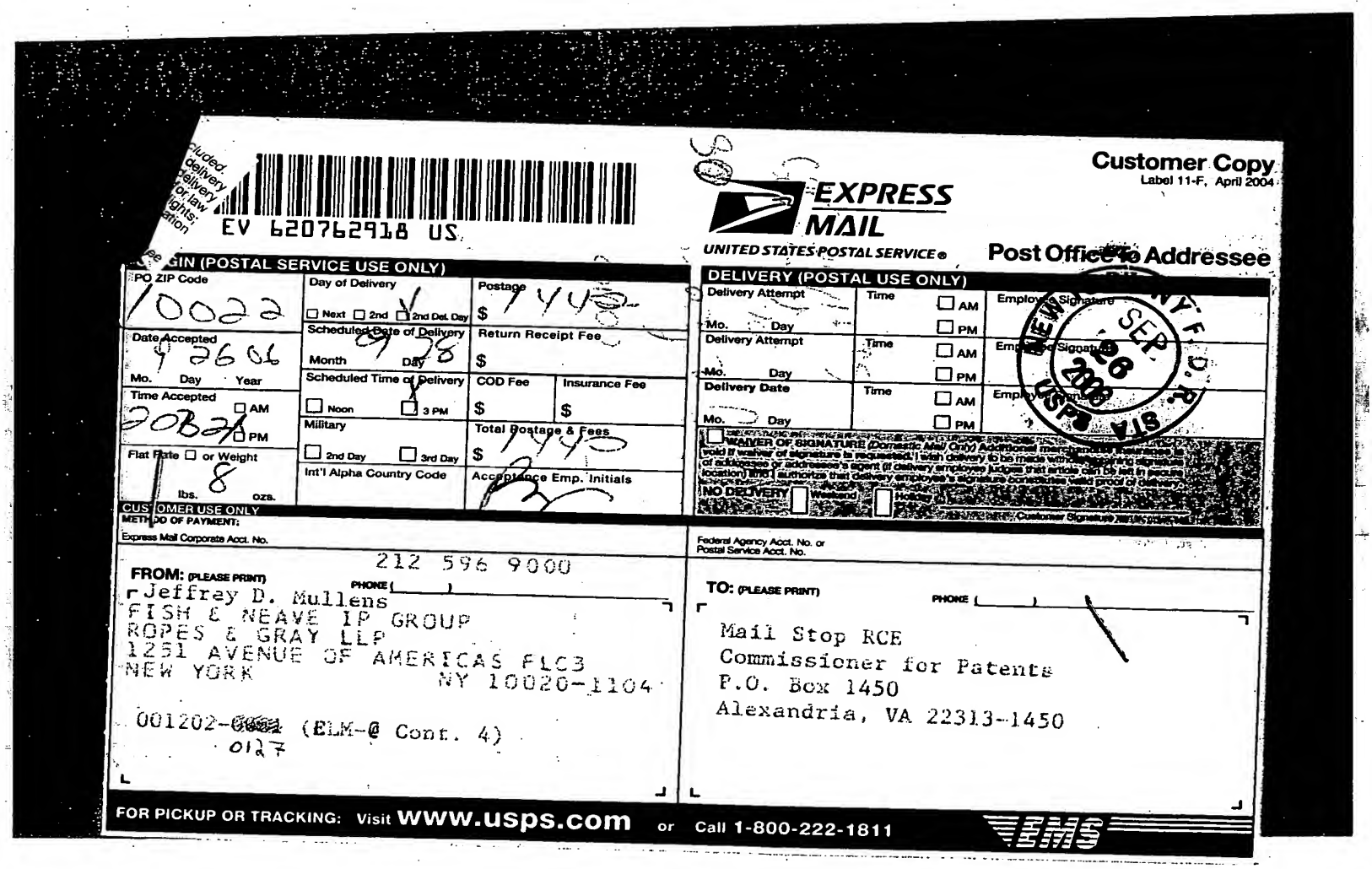
COMMISSIONER FOR PATENTS

JDM/TBD/kl 001202-0127

Express Mail Label No. EV620762918US

Appendix B

Copy of an Express Mail mailing label date-stamped by the USPS on September 26, 2006 and having the Express Mail number indicated on applicant's submissions of September 26, 2006.



EV 620762918 US

EXPRESS MAIL
UNITED STATES POSTAL SERVICE®

Customer Copy
Label 11-F, April 2004

Post Office to Addressee

ORIGIN (POSTAL SERVICE USE ONLY)

PO ZIP Code: 10022
Day of Delivery: ☐ Next ☐ 2nd ☐ 2nd Del. Day
Postage: $ 19.45
Date Accepted: 9 26 06 (Mo. Day Year)
Scheduled Date of Delivery: Month 9 Day 28
Return Receipt Fee: $
Time Accepted: 2082 ☐ AM ☐ PM
Scheduled Time of Delivery: ☐ Noon ☐ 3 PM
COD Fee: $
Insurance Fee: $
Flat Rate ☐ or Weight: 8 lbs. oz.
Military: ☐ 2nd Day ☐ 3rd Day
Total Postage & Fees: $ 19.45
Int'l Alpha Country Code
Acceptance Emp. Initials

DELIVERY (POSTAL USE ONLY)

Delivery Attempt: Mo. Day — Time ☐ AM ☐ PM — Employee Signature
Delivery Attempt: Mo. Day — Time ☐ AM ☐ PM — Employee Signature
Delivery Date: Mo. Day — Time ☐ AM ☐ PM — Employee Signature

SEP 28 2006 USPS

☐ WAIVER OF SIGNATURE (Domestic Mail Only) Additional merchandise insurance is void if waiver of signature is requested. I wish delivery to be made without obtaining signature of addressee or addressee's agent (if delivery employee judges that article can be left in secure location) and authorize that delivery employee's signature constitutes valid proof of delivery.
NO DELIVERY ☐ Weekend ☐ Holiday

Customer Signature

CUSTOMER USE ONLY
METHOD OF PAYMENT:
Express Mail Corporate Acct. No.
Federal Agency Acct. No. or Postal Service Acct. No.

FROM: (PLEASE PRINT) PHONE (212 596 9000)
Jeffrey D. Mullens
FISH & NEAVE IP GROUP
ROPES & GRAY LLP
1251 AVENUE OF AMERICAS FLC3
NEW YORK NY 10020-1104

001202-0127 (ELM-@ Cont. 4)

TO: (PLEASE PRINT) PHONE ( )
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FOR PICKUP OR TRACKING: Visit www.usps.com or Call 1-800-222-1811

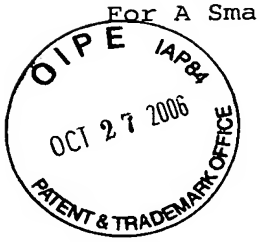
EMS

Appendix C

Copies of an Express Mail Certification, Request for Continued Examination, Petition for Extension of Time, Reply to Office Action, and Information Disclosure Statement filed by the applicant on September 26, 2006.

Rev. 12/04
For A Small Entity

PATENTS



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. ELM-2 Cont. 4

Examiner Monica Lewis
Art Unit 2822

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

EXPRESS MAIL CERTIFICATION

"Express Mail" mailing label number EV620762918US
Date of Deposit September 26, 2006.

I hereby certify that this transmittal letter and the other papers identified in this transmittal letter as being transmitted herewith are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and are addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Isatta B. Smith

REQUEST FOR CONTINUED EXAMINATION

Sir:

This is a request for continued examination under 37 C.F.R. § 1.114, of pending prior Application No. 10/672,961 (Confirmation No. 9439), filed on September 26, 2003 of Glenn J. Leedy for THREE DIMENSIONAL MULTI LAYER MEMORY AND CONTROL LOGIC INTEGRATED CIRCUIT STRUCTURE.

1. ☐ Please enter the Amendment Pursuant to 37 C.F.R. § 1.116 filed on _____ in Application No. _____.

2. ☐ Please consider the arguments in the Appeal Brief or Reply Brief filed on _____ in Application No. _____.

3. ☒ A Reply to an Office Action is enclosed.

4. ☐ Affidavit(s)/Declaration(s) is/are enclosed.

5. ☒ An Information Disclosure Statement (in duplicate) is enclosed, including a Form PTO/SB/08 (in duplicate) and copies of thirteen (13) cited references.

6. ☐ A suspension of action on the above-identified patent application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months.

7. ☐ A check in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(e) is enclosed.

8. ☒ Please charge $ 395.00 to Deposit Account No. 06-1075 (Order No. 001202-0127) in payment of the fee under 37 C.F.R. § 1.17(e). A duplicate copy of this Request is enclosed.

9. FEE FOR ADDITIONAL CLAIMS

[X] A fee for additional claims is not required.

[ ] A fee for additional claims is required.

The additional fee has been calculated as shown below:

	Claims Remaining After Amendment		Highest Number Previously Paid for	Present Extra	Rate	Fees
TOTAL CLAIMS	41	-	41*	=	x $25	= $ 0.00
INDEPENDENT CLAIMS	3	-	3**	=	x $100	= $ 0.00
FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $180	= $ 0.00
* If less than 20, insert 20.					TOTAL	$ 0.00
** If less than 3, insert 3.						

10. ☐ The Director is hereby authorized to charge payment of $ _____ in payment of the fee for additional claims, and to charge any additional fees required under 37 C.F.R. § 1.17(e) in connection with this Request, or to credit any overpayment of same, to Deposit Account No. 06-1075. A duplicate copy of this Request is enclosed.

11. ☒ Please grant a ☐ one-month, ☐ two-month, ☒ three-month, ☐ four-month, extension of time under 37 C.F.R. § 1.136(a) to the Examiner's Action of March 28, 2006 in the above-identified patent application. With the the extension, the time for replying is extended up to an including September 28, 2006.

12. ☐ The appropriate fee for a -month extension of time to respond to the final rejection was timely paid on _____.

13. ☐ An additional ___-month extension of time to respond to the final rejection is requested.

14. ☐ A check in the amount of $ _____ in payment of the extension-of-time fee is enclosed.

15. ☒ Please charge the extension-of-time fee of $ 510.00 to Deposit Account No. 06-1075 (Order No. 001202-0127). A duplicate copy of this Request is enclosed.

16. ☒ The Director is hereby authorized to charge payment of any additional fees required under 37 C.F.R. § 1.16 or § 1.17 in connection with this paper, or to credit any overpayment of same, to Deposit Account No. 06-1075 (Order No. 001202-0127). A duplicate copy of this Request is enclosed.

September 26, 2006
(Date)

Jeffrey C. Aldridge
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EXPRESS MAIL LABEL NO. EV620762918US

PATENTS
ELM-2 Cont. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicant : Glenn J. Leedy

Application No. : 10/672,961 Confirmation No. : 9439

Filed : September 26, 2003

For : THREE DIMENSIONAL MULTI LAYER MEMORY AND CONTROL LOGIC INTEGRATED CIRCUIT STRUCTURE

Art Unit : 2822

Examiner : Monica Lewis

New York, NY 10020
September 26, 2006

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

REPLY TO OFFICE ACTION

Sir:

In reply to the March 28, 2006 Office Action, applicant hereby amends the above-identified patent application as follows:

Amendments to the Claims begin on page 2 of this Reply.

Remarks begin on page 14 of this Reply.

Amendments to the claims

The following listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1-87. (Canceled)

88. (Currently amended) An integrated circuit structure comprising:

a first substrate comprising a first surface having interconnect contacts formed thereon; and

a second substrate comprising a first surface having interconnect contacts formed thereon, the first surface of the second substrate being bonded to the first surface of the first substrate to form conductive paths between the interconnect contacts of the first ~~substrate~~ surfaces of the first and ~~the~~ second ~~substrate~~ substrates, wherein the second substrate is a thinned substrate having circuitry formed thereon.

89. (Withdrawn) The apparatus of claim 88, wherein the second substrate is one of a thinned monocrystalline semiconductor substrate and a thinned polycrystalline semiconductor substrate.

90. (Withdrawn) The apparatus of claim 88, wherein the circuitry formed on the second substrate is one of active circuitry and passive circuitry.

91. (Withdrawn) The apparatus of claim 88, wherein the circuitry formed on the second substrate consists of both active circuitry and passive circuitry.

92. (Withdrawn) The apparatus of claim 88, wherein the first substrate is a substrate having circuitry formed thereon.

93. (Withdrawn) The apparatus of claim 92, wherein the circuitry of the first substrate is one of active circuitry and passive circuitry.

94. (Withdrawn) The apparatus of claim 92, wherein the circuitry of the first substrate comprises both active circuitry and passive circuitry.

95. (Previously presented) The structure of claim 88, further comprising:

at least one additional thinned substrate having circuitry formed thereon;

a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent additional thinned substrate; and

conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated circuit structure.

96. (Withdrawn) The apparatus of claim 95, wherein at least two of the first, the second and the at least one additional thinned substrates are formed using a different process technology, wherein the different process technology is selected from the group consisting of DRAM, SRAM, FLASH, EPROM, EEPROM, Ferroelectric and Giant Magneto Resistance.

97. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second and the at least one additional thinned substrates comprises a microprocessor.

98. (Withdrawn) The apparatus of claim 95, wherein:

at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon; and

at least one substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs tests on the at least one substrate that has memory circuitry formed thereon.

99. (Withdrawn) The apparatus of claim 95, wherein at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations, wherein at least one memory location of the plurality of memory locations is used for sparing and wherein data from the at least one memory location on the at least one substrate having memory circuitry formed thereon is used instead of data from a defective memory location on the at least one substrate that has memory circuitry formed thereon.

100. (Withdrawn) The apparatus of claim 95, wherein:

at least one substrate of the first, the second and the at least one additional thinned substrates has

memory circuitry formed thereon; and

at least one substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs programmable gate line address assignment with respect to the at least one substrate having memory circuitry formed thereon.

101. (Withdrawn) The apparatus of claim 95, further comprising a plurality of interior vertical interconnections that traverse at least one of the first, the second and the at least one additional thinned substrates.

102. (Withdrawn) The apparatus of claim 95, wherein information processing is performed on data routed between the circuitry of at least two of the first, the second and the at least one additional thinned substrates.

103. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second and the at least one additional thinned substrates has reconfiguration circuitry.

104. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second, and the at least one additional thinned substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

105. (Withdrawn) The apparatus of claim 95, further comprising:

a memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores a data value and has circuitry for coupling the data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines;

circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and

a controller that determines if one of the plurality of memory cells is defective and alters said mapping to remove references to the one of the plurality of memory cells that is defective.

106. (Previously presented) The structure of claim 95, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address

assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

107. (Previously presented) The structure of claim 106, wherein the controller substrate logic:

tests the array of memory cells periodically to determine if one of the array of memory cells is defective; and

removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

108. (Previously presented) The structure of claim 106, further comprising:

programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

109. (Previously presented) The structure of claim 106, wherein the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the

physical order of at least one memory cell is different than the logical order of the at least one memory cell.

110. (Previously presented) The structure of claim 106, wherein:

the logic circuitry of the at least one controller substrate is tested by an external means; and

the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate, wherein the testing achieves a functional testing of a substantial portion of the array of memory cells.

111. (Previously presented) The structure of claim 106, wherein the logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

112. (Previously presented) The structure of claim 106, wherein the controller substrate logic is further configured to:

prevent the use of at least one defective gate line; and

replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

113. (Previously presented) The structure of claim 106, wherein the controller substrate logic is further configured to prevent the use of at least one defective gate line.

114. (Previously presented) The structure of claim 106, wherein the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

115. (Withdrawn) The apparatus of claim 88, wherein the first substrate is a non-semiconductor material.

116. (Currently amended) An integrated circuit structure comprising:

a first substrate[[,]] having topside and ~~backside~~ bottomside surfaces, the topside surface of the first substrate having interconnect contacts formed thereon;

a second substrate[[,]] having topside and ~~backside~~ bottomside surfaces, the bottomside surface of the second substrate having interconnect contacts formed thereon and being bonded to the topside surface of the first substrate; and

conductive paths formed between the interconnect contacts on ~~selected ones of said surfaces of said substrates, so as to form~~ the topside of the first substrate and on the bottomside of the second substrate, the conductive paths providing electrical connections between the first substrate and the second substrate, wherein the second substrate is a thinned substrate having circuitry formed thereon.

117. (Currently amended) The integrated circuit structure of claim 116, wherein selected ones of said ~~conductive paths~~ interconnect contacts on ~~one~~ said topside

surface of said first substrate are in ~~physical and thus~~ electrical contact with selected ones of the ~~conductive paths~~ interconnect contacts on ~~one~~ said bottomside surface of said second substrate so as to form said electrical connections.

118. (Currently amended) An integrated circuit structure comprising:

a first substrate;

a second substrate bonded to the first substrate, wherein the first substrate has a first surface bonded to a first surface of the second substrate and wherein ~~said~~ the first and second substrates ~~having~~ have ~~bonded surfaces and opposite~~ second surfaces opposite to ~~of~~ said ~~bonded~~ first surfaces; and

conductive paths formed ~~between~~ on the first surfaces of the first ~~substrate~~ and ~~the~~ second ~~substrate from selected ones of said surfaces of said~~ substrates, wherein the second substrate is a thinned substrate having circuitry formed thereon.

119. (Previously presented) The structure of claim 116, further comprising:

at least one additional thinned substrate having circuitry formed thereon;

a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent additional thinned substrate; and

conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between

each additional thinned substrate and at least one of said substrates of the integrated circuit structure.

120. (Previously presented) The structure of claim 119, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

121. (Previously presented) The structure of claim 120, wherein the controller substrate logic:

tests the array of memory cells periodically to determine if one of the array of memory cells is defective; and

removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

122. (Previously presented) The structure of claim 120, further comprising:

programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

123. (Previously presented) The structure of claim 120, wherein the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

124. (Previously presented) The structure of claim 120, wherein:

the logic circuitry of the at least one controller substrate is tested by an external means; and

the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate, wherein the testing achieves a functional testing of a substantial portion of the array of memory cells.

125. (Previously presented) The structure of claim 120, wherein the logic circuitry of the at least one

controller substrate performs functional testing of a substantial portion of the array of memory cells.

126. (Previously presented) The structure of claim 120, wherein the controller substrate logic is further configured to:

prevent the use of at least one defective gate line; and

replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

127. (Previously presented) The structure of claim 120, wherein the controller substrate logic is further configured to prevent the use of at least one defective gate line.

128. (Previously presented) The structure of claim 120, wherein the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

REMARKS/ARGUMENTS

Summary of Office Action

Claims 88-128 are pending. Of these, claims 89-94, 96-105, and 115 are withdrawn.

The information disclosure statement filed on December 23, 2005 was objected to for failing to comply with 37 C.F.R. §1.98(a)(2) in failing to include legible copies of each cited foreign patent document and non-patent literature publication.

Claim 88 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of Leedy U.S. Patent No. 6,563,224 (hereinafter "the '224 patent").

Claim 117 was rejected under 35 U.S.C. § 112 for allegedly containing subject matter which was not described in the specification.

Claims 88, 95, 116, 118, and 119 were rejected under 35 U.S.C. § 102(b) as anticipated by Faris U.S. Patent No. 5,786,629 (hereinafter "Faris").

Claims 106-108, 111-114, 120-122, and 125-128 were rejected under 35 U.S.C. § 103(a) as being obvious from Faris in view of Sakui et al. U.S. Patent No. 5,615,163 (hereinafter "Sakui"). Claims 109 and 123 were rejected under 35 U.S.C. § 103(a) as being obvious from Faris in view of Daberko U.S. Patent No. 5,787,445 (hereinafter "Daberko"). Claim 117 was rejected under 35 U.S.C. § 103(a) as being obvious from Faris in view of Pamler et al. U.S. Patent No. 5,626,279 (hereinafter "Pamler").

Claims 110 and 124 were objected to for being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Summary of Applicant's Amendments

Applicant notes with appreciation the indication of allowable subject matter in claims 110 and 124. Applicant reserves the right to re-write claims 110 and 124 in independent form.

Applicant has amended claims 88, 116, 117, and 118 to more particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner's objections and rejections are respectfully traversed.

Applicant's Reply to the Objection to the Information Disclosure Statement

The Examiner objected to the Information Disclosure Statement filed December 23, 2005 for failing to comply with 37 C.F.R. §1.98(a)(2) in failing to include legible copies of each cited foreign patent document and non-patent literature publication.

Applicant is filing herewith an IDS re-citing and enclosing copies of the Svechnikov, Salazar, Allen and Kochugova non-patent literature publications which were not initialed by the Examiner on the copy of the December 23, 2005 Form PTO/SB/08 returned with the last communication.

The Double Patenting Rejection of Claim 88

Claim 88 was rejected under the judicially created doctrine of obviousness-type double patenting as

being unpatentable over claim 1 of Leedy U.S. Patent No. 6,563,224 (hereinafter "the '224 patent").

Applicant traverses the Examiner's rejection and submits that claim 1 of the '224 patent includes a memory circuit and applicant's amended claim 88 does not. Since a memory circuit having a thinned substrate of claim 1 of the '224 patent is patentably distinct from an integrated circuit of applicant's amended independent claim 88, the double patenting rejection should be withdrawn.

Additionally, applicant submits that claim 1 of the '224 patent includes conductive paths between a first substrate and a second substrate and applicant's amended claim 88 requires conductive paths between interconnect contacts of first surfaces of first and second substrates. Since conductive paths between substrates as required by claim 1 of the '224 patent are patentably distinct from conductive paths between interconnect contacts as required by applicant's amended claim 88, the double patenting should be withdrawn.

Regardless, applicant notes that claim 88 is still rejected under 35 U.S.C. § 102(b) as being anticipated by Faris. As discussed below, amended claim 88 is allowable over Faris. If the Examiner does not withdraw the 102(b) rejection in view of Faris, however, applicant may decide to further amend claim 88 in order to expedite prosecution. Further amendments to claim 88 may remove the Examiner's double patenting rejection and the corresponding request that a Terminal Disclaimer be filed. Thus, applicant respectfully submits that the Examiner's double patenting rejection is premature.

The Rejections of Claims 88, 95, 106-109, 111-114, 116-123 and 125-128

Claims 88, 95, 116, 118, and 119 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Faris. Claims 106-108, 111-114, 120-122, and 125-128 were rejected under 35 U.S.C. § 103(a) as being obvious from Faris in view of Sakui. Claims 109 and 123 were rejected under 35 U.S.C. § 103(a) as being obvious from Faris in view of Daberko. Claim 117 was rejected under 35 U.S.C. § 103(a) as being obvious from Faris in view of Pamler.

Claim 88

Amended claim 88 is directed to an integrated circuit structure including a first and a second substrate. The first and second substrates each include a first surface having interconnect contacts formed thereon. The second substrate has its first surface bonded to the first surface of the first substrate to form conductive paths between the interconnect contacts of the first surfaces of the first and second substrates. The second substrate is a thinned substrate having circuitry formed thereon.

Faris discusses a three-dimensional package including a large number of fillo-leaf subassemblies bonded together at one of their edges. Encoder lines in the subassemblies terminate at the bonded outer edge of the subassemblies, and interconnections formed on the bonded outer edge provide connections between the subassemblies and further circuitry.

The Examiner contends that Faris describes applicant's claimed invention (Office Action, page 4). Faris, however, does not show or suggest first surfaces of first and second substrates having interconnect contacts

formed thereon, the first surfaces being bonded to each other to form conductive paths between the interconnect contacts, as recited in claim 88. At best, Faris discusses connections formed on the outer edge of substrates to provide connections to the subassemblies. Connections formed on an outer edge are not interconnections located on first surfaces of substrates that are bonded to each other, as included in applicant's amended claim 88.

For at least the above reasons, applicant respectfully submits that amended independent claim 88 and any claims which depend therefrom, including claims 95, 106-109 and 111-115, are allowable.

Claim 116

Amended claim 116 is directed to an integrated circuit structure including first and second substrates each having topside and bottomside surfaces. The topside surface of the first substrate and the bottomside of the second substrate have interconnect contacts formed thereon and are bonded to each other. Conductive paths are formed between the interconnect contacts on the topside of the first substrate and the bottomside of the second substrate, the conductive paths providing electrical connections between the first and second substrates. The second substrate is a thinned substrate having circuitry formed thereon.

As discussed above in connection with claim 88, applicant submits that Faris does not show or suggest topside and bottomside surfaces of first and second substrates, respectively, having interconnect contacts formed thereon, the topside and bottomside surfaces being bonded to each other, and conductive paths formed between

the topside and bottomside surfaces for providing electrical connections between the substrates, as recited in claim 116. At best, Faris discusses connections formed on the outer edge of substrates to provide connections to the subassemblies. Connections formed on an outer edge are not interconnections formed between contacts located on first surfaces that are bonded to each other, as included in applicant's amended claim 116.

For at least the above reasons, applicant respectfully submits that amended independent claim 116 and any claims which depend therefrom, including claims 117, 119-123, and 125-128, are allowable.

Claim 118

Amended claim 118 is directed to an integrated circuit structure including a first substrate and a second substrate bonded to the first substrate. The first substrate and the second substrate have first surfaces that are bonded to each other and that have conductive paths formed thereon. The second substrate is a thinned substrate having circuitry formed thereon.

As discussed above in connection with claim 88, applicant submits that Faris does not show or suggest first surfaces of first and second substrates having conductive paths formed thereon and being bonded to each other, as recited in claim 118. At best, Faris discusses substrates having conductive lines formed on one of their surfaces, the substrates being bonded to each other in a stack such that a surface having a conductive line of a substrate is bonded to a surface not having a conductive line of another substrate (see Faris, FIGS. 4-5). The substrates of Faris are stacked such that surfaces of substrates having

conductive lines thereon do not face each other in the stack. For at least the reason that applicant's amended claim 118 requires that the first surfaces of the first and second substrates have conductive paths formed thereon that are bonded to each other, applicant respectfully submits that amended independent claim 118 is allowable. Accordingly, applicant respectfully requests that the Examiner's rejection of claim 118 in view of Faris be withdrawn.

Withdrawn Claims

Applicant would like to point out that claims 89-94, 96-105, and 115, which depend from claim 88, are withdrawn. Once claim 88 is allowed, withdrawn dependent claims 89-94, 96-105, and 115 should be reinstated and allowed.

Conclusion

The foregoing demonstrates that claims 88, 95, 106-114, 116-128, and any claims dependent therefrom are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

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EXPRESS MAIL LABEL NO. EV620762918US

PATENTS
Attorney Docket No.: ELM-2 Cont. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Glenn J. Leedy
Application No.	:	10/672,961 Confirmation No.: 9439
Filed	:	September 26, 2003
For	:	THREE DIMENSIONAL MULTI LAYER MEMORY AND CONTROL LOGIC INTEGRATED CIRCUIT STRUCTURE
Group Art Unit	:	2822
Examiner	:	Monica Lewis

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicant wishes to call the attention of the Examiner to the following documents:

U.S. Patent Documents

US 3,636,358	01/18/1972	Groschwitz	(6)
US 3,932,932	01/20/1976	Goodman	(2)
US 4,028,547	06/07/1977	Eisenberger	(3)
US 4,393,127	07/12/1983	Greschner et al.	(3)
US 4,528,072	07/09/1985	Kurosawa et al.	(2)
US 4,566,037	01/21/1986	Takatsu et al.	(6)
US 4,622,632	11/11/1986	Tanimoto et al.	(6)
US 4,810,889	03/07/1989	Yokomatsu et al.	(3)
US 5,051,326	09/24/1991	Celler et al.	(3)
US 5,062,689	11/05/1991	Koehler	(8)
US 5,117,282	05/26/1992	Salatino	(7)
US 5,166,962	11/24/1992	Murooka et al.	(3)

U.S. Patent Documents

US 5,169,805	12/08/1992	Mok et al.	(4)
US 5,188,706	02/23/1993	Hori et al.	(3)
US 5,245,277	09/14/1993	Furtek et al.	(6)
US 5,283,107	02/01/1994	Bayer et al.	(6)
US 5,293,457	03/08/1994	Arima et al.	(6)
US 5,399,505	03/21/1995	Dasse et al.	(6)
US 5,432,999	07/18/1995	Capps et al.	(5)
US 5,450,603	09/12/1995	Davies	(6)
US 5,517,457	05/14/1996	Sakui et al.	
US 5,572,689	11/05/1996	Gallup et al.	(6)
US 6,017,658	01/25/2000	Rhee et al.	(9)
US 6,092,174	07/18/2000	Roussakov	(6)
US 6,154,809	11/28/2000	Ikenaga et al.	(6)
US 6,300,935	10/09/2001	Sobel et al.	(6)
US 6,301,653	10/09/2001	Mohamed et al.	(6)
US 6,320,593	11/20/2001	Sobel et al.	(6)
US 6,355,976	03/12/2002	Faris	
US 2005-0023656	02/03/2005	Leedy	(6)
US 6,894,392	05/17/2005	Gudesen et al.	(6)

Foreign Patent Documents

DE 3233195	03/17/1983	Mitsubishi Electric Corporation
JP 2037655	02/07/1990	Siemens AG
JP 3127816	05/30/1991	Canon KK
JP 3174715	07/29/1991	Fujitsu Limited
WO 98/19337	05/07/1998	Trusi Technologies, LLC

Nonpatent Literature Documents

Wolf, Stanley and Richard N. Tauber; Silicon Procesing For the VLSI Era, Volume 1: Process Technology; Sunset Beach, CA: Lattice Press, 1986, pages 191-194 (6)

European Search Report for Application No. EP 02 00 9643 (date completed: October 8, 2002)

Phys. Rev. B., Condens. Matter Mater. Phys. (USA), Physical Review B (Condensed Matter and Materials Physics), 15 March 2003, APS through AIP, USA.

S. Wolf, Silicon Processing For the VLSI Era, 1990, Lattice Press, Volume 2, page 191. (10)

Nonpatent Literature Documents

Svechnikov, S.V.; Kobylyatskaya, M.F.; Kimarskii, V.I.; Kaufman, A.P.; Kuzolev, Yu. I.; Cherepov, Ye. I.; Fomin, B.I.; "A switching plate with aluminium membrane crossings of conductors"; 1972 *(1)*

Salazar, M.; Wilkins, C.W., Jr.; Ryan, V.W.; Wang, T.T.; "Low stress films of cyclized polybutadiene dielectrics by vacuum annealing"; Oct. 21-22, 1986; pp. 96-102. *(1)*

Allen, Mark G.,: Senturia, Stephen D.; "Measurement of polymide interlayer adhesion using microfabricated structures"; 1988; pp. 352-356. *(1)*

Kochugova, I.V.; Nikolaeva, L.V.; Vakser, N.M., (M.I. Kalinin Leningrad Polytechnic Institute (USSR); "Electrophysical investigation of thin-layered inorganic coatings"; 1989; pp. 826-828. *(1)*

The aforementioned references are listed on the accompanying Form PTO/SB/08 (submitted in duplicate). Pursuant to 37 C.F.R. 1.98 (a)(2), applicant is not submitting copies of the aforementioned U.S. patent document references. Copies of the aforementioned Foreign Patent Documents and Non-Patent Literature Documents are enclosed herewith.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

The above-identified Non-Patent Literature Documents identified by *(1)* were previously cited in an Information Disclosure Statement filed on December 23, 2005, and were not considered by the Examiner. These references

are being re-submitted herewith for the Examiner's consideration.

The aforementioned documents identified by *(2)* were cited in an Office Action mailed on November 17, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/742,057. Documents identified by *(3)* were cited in an Office Action mailed on December 7, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/766,557. The Document identified by *(4)* was cited in an Office Action mailed on December 13, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/742,282. The document identified by *(5)* was cited in an Office Action mailed on December 19, 2005 in co-pending commonly assigned U.S. Patent Application No. 10/379,820. The U.S. Patent Documents and Nonpatent Literature Documents identified by *(6)* were cited in an Office Action mailed on January 26, 2006 in co-pending commonly assigned U.S. Patent Application No. 10/741,647. The aforementioned document identified by *(7)* was cited in an Office Action mailed in co-pending commonly assigned U.S. Patent Application No. 10/742,057 on May 18, 2006; the document identified by *(8)* was cited in an Office Action mailed in co-pending commonly assigned U.S. Patent Application No. 10/385,386 on April 26, 2006; the document identified by *(9)* was cited in an Office Action mailed in co-pending commonly assigned U.S. Patent Application No. 10/766,557 on June 5, 2006; the document identified by *(10)* was cited in an Office Action mailed in co-pending commonly assigned U.S. Patent Application No. 10/379,820 on April 20, 2006.

It is respectfully requested that these references be: (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed

on any patent which may issue on this application. Applicant requests that a copy of Form PTO-SB/08, as considered and initialed by the Examiner, be returned with the next communication.

This Statement is submitted with a Request for Continued Examination under 37 C.F.R. § 1.114. The Director is hereby authorized to charge $180.00 in payment of the fee for submission of this Information Disclosure Statement pursuant to 37 C.F.R. §1.97(c)(2), payment of any additional fees required in connection with this Statement, or to credit any overpayment of the same, to Deposit Account No. 06-1075 (Order No.: 001202-0127). A duplicate copy of this Information Disclosure Statement is enclosed herewith.

An early and favorable action is respectfully requested.

Respectfully submitted,

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PTO/SB/08a/b (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/672,961 (Conf. No. 9439)
Filing Date	September 26, 2003
First Named Inventor	Glenn J. Leedy
Art Unit	2822
Examiner Name	Monica Lewis
Attorney Docket Number	ELM-2 Cont. 4

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 3,636,358	01/18/1972	Groschwitz	
		US 3,932,932	01/20/1976	Goodman	
		US 4,028,547	06/07/1977	Eisenberger	
		US 4,393,127	07/12/1983	Greschner et al.	
		US 4,528,072	07/09/1985	Kurosawa et al.	
		US 4,566,037	01/21/1986	Takatsu et al.	
		US 4,622,632	11/11/1986	Tanimoto et al.	
		US 4,810,889	03/07/1989	Yokomatsu et al.	
		US 5,051,326	09/24/1991	Celler et al.	
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		US 5,117,282	05/26/1992	Salatino	
		US 5,166,962	11/24/1992	Murooka et al.	
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		US 5,188,706	02/23/1993	Hori et al.	
		US 5,245,277	09/14/1993	Furtek et al.	
		US 5,283,107	02/01/1994	Bayer et al.	
		US 5,293,457	03/08/1994	Arima et al.	
		US 5,399,505	03/21/1995	Dasse et al.	
		US 5,432,999	07/18/1995	Capps et al.	
		US 5,450,603	09/12/1995	Davies	
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		US 5,572,689	11/05/1996	Gallup et al.	
		US 6,017,658	01/25/2000	Rhee et al.	
		US 6,092,174	07/18/2000	Roussakov	
		US 6,154,809	11/28/2000	Ikenaga et al.	
		US 6,300,935	10/09/2001	Sobel et al.	
		US 6,301,653	10/09/2001	Mohamed et al.	
		US 6,320,593	11/20/2001	Sobel et al.	
		US 6,355,976	03/12/2002	Faris	
		US 2005-0023656	02/03/2005	Leedy	
		US 6,894,392	05/17/2005	Gudesen et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		DE3233195	03-17-1983	Mitsubishi Electric Corp.		
		JP2037655	02-07-1990	Siemens AG		
		JP3127816	05-30-1991	Canon KK		
		JP3174715	07-29-1991	Fujitsu Limited		
		WO 98/19337	05-07-1998	Trusi Technologies, LLC		

Examiner Signature		Date Considered	

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PTO/SB/08a/b (08-03)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/672,961 (Conf. No. 9439)
Filing Date	September 26, 2003
First Named Inventor	Glenn J. Leedy
Art Unit	2822
Examiner Name	Monica Lewis
Attorney Docket Number	ELM-2 Cont. 4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Wolf, Stanley and Richard N. Tauber; Silicon Processing For the VLSI Era, Volume 1: Process Technology; Sunset Beach, CA: Lattice Press, 1986, pages 191-194	
		European Search Report for Application No. EP 02 00 9643 (date completed: October 8, 2002)	
		Phys. Rev. B., Condens. Matter Mater. Phys. (USA), Physical Review B (Condensed Matter and Materials Physics), 15 March 2003, APS through AIP, USA.	
		S. Wolf, Silicon Processing For the VLSI Era, 1990, Lattice Press, Volume 2, page 191.	
		Svechnikov, S.V.; Kobylyatskaya, M.F.; Kimarskii, V.I.; Kaufman, A.P.; Kuzolev, Yu. I.; Cherepov, Ye. I.; Fomin, B.I.; "A switching plate with aluminium membrane crossings of conductors";1972	
		Salazar, M.; Wilkins, C.W., Jr.; Ryan, V.W.; Wang, T.T.; "Low stress films of cyclized polybutadiene dielectrics by vacuum annealing"; Oct. 21-22, 1986; pp. 96-102.	
		Allen, Mark G.,: Senturia, Stephen D.; "Measurement of polymide interlayer adhesion using microfabricated structures"; 1988; pp. 352-356.	
		Kochugova, I.V.; Nikolaeva, L.V.; Vakser, N.M., (M.I. Kalinin Leningrad Polytechnic Institute (USSR); "Electrophysical investigation of thin-layered inorganic coatings"; 1989; pp. 826-828.	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	

Appendix D

Copy of the front page of applicant's Reply to Office Action of September 26, 2006 as downloaded from PAIR.

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PATENTS
ELM-2 Cont. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicant	:	Glenn J. Leedy
Application No.	:	10/672,961 Confirmation No. : 9439
Filed	:	September 26, 2003
For	:	THREE DIMENSIONAL MULTI LAYER MEMORY AND CONTROL LOGIC INTEGRATED CIRCUIT STRUCTURE
Art Unit	:	2822
Examiner	:	Monica Lewis

New York, NY 10020
September 26, 2006

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

REPLY TO OFFICE ACTION

Sir:

In reply to the March 28, 2006 Office Action, applicant hereby amends the above-identified patent application as follows:

Amendments to the Claims begin on page 2 of this Reply.

Remarks begin on page 14 of this Reply.

PTO/SB/92 (09-06)
Approved for use through 03/31/2007. OMB 0561-0031
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Attorney Docket No. ELM-2 CONT. 4

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Date of Deposit: October 27, 2006

I hereby certify that this paper/fee and all enclosures noted below are being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" under 37 C.F.R. § 1.10 on the dated indicated above and is addressed to:

Director of the U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

1. Petition under 37 C.F.R. §1.181(a) to Withdraw Holding of Abandonment Based on Evidence that a Reply Was Timely Mailed or Filed (in duplicate);
2. Appendix A - Copy of a return receipt postcard itemizing the submissions made by applicant on September 26, 2006 and date-stamped by the Patent and Trademark Office on September 26, 2006;
3. Appendix B - Copy of an Express Mail mailing label date-stamped by the USPS on September 26, 2006 and having the Express Mail number indicated on applicant's submissions of September 26, 2006;
4. Appendix C - Copies of an Express Mail Certification, Request for Continued Examination, Petition for Extension of Time, Reply to Office Action, and Information Disclosure Statement filed by the applicant on September 26, 2006;
5. Appendix D - Copy of the front page of applicant's Reply to Office Action of September 26, 2006 as downloaded from PAIR.; and
6. Return Postcard.

Rose Marie Dhanraj

Signature

ROSE MARIE DHANRAJ

Typed or printed name of person signing Certificate

N/A	212.596.9000
Registration Number, if applicable	Telephone Number

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.